

# Characterization of an Ultra-Thick Positive Photoresist for Electroplating Applications

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The performance requirements for ultra-thick photoresists are rapidly increasing with the dramatic growth in new lithographic applications that require electroplating processes. Two of the main applications for ultra-thick photoresists are nanotechnology (MEMS) and advanced packaging. Flipchip packaging has become widely adopted to address electrical device performance and chip form factor considerations. The growth in the nanotechnology market is driven by a wide range of products, which include accelerometers, ink jet print heads, biomedical sensors and optical switches.

Electroplating levels for these applications require a photosensitive polymer material capable of coating, exposing and plating with conventional semiconductor equipment and standard ancillary process chemicals. A single coat step to achieve the final photoresist thickness is critical to minimize the number of process steps and cycle time. For this thick layer the sidewall profile, aspect ratio, electroplating durability and subsequent stripability are all important. This study characterized a novel positive photoresist (Shin-Etsu SIPR<sup>®</sup>) for use in a 100 micron thick coat for electroplating on copper.

The lithographic performance of the ultra-thick positive photoresist was optimized using a broad band, 1X KARL SUSS MA150 aligner used in the proximity mode. All proximity gaps were hard set at 100 microns. Cross sectional SEM analysis, process linearity, and optimized proximity gaps were used to establish the lithographic capabilities. High aspect ratio structures were then electroplated using the optimized photoresist process to demonstrate photoresist durability and stripability. A recommended process flow is described for this photoresist and exposure tool.

**Key Words:** advanced packaging, MEMS, thick resist, electroplating, process optimization, Cu bump, single coat 100 micron resist film

## 1.0 INTRODUCTION

Recently there has been a rapid acceleration in the pace of conversion from conventional ceramic and plastic based integrated circuit (IC) packaging to advanced wafer level chip scale packaging, primarily using copper and solder bump technology. Initially driven by the need for smaller form factors for cellular telephones and other portable electronic devices, there is a growing dependency on increased signal speed and very high input/output (I/O) counts in a widening range of IC types that cannot be adapted to conventional packaging. As fabrication processes transition from 200 mm to 300 mm Silicon wafers and

compound semiconductors, it is anticipated that 50 to 65 percent of the devices will be processed with advanced wafer level packaging [2].

The conversion to advanced packaging for more complex ICs is accelerating the technology to a tighter solder ball pitch to accommodate higher I/O density [3]. One solution is the use of thicker photoresists that allow sufficient copper bump height to eliminate underfill technology. The taller bumps allow the over mold compound to create a void free fill, thus eliminating a process step. In this application the photoresist thickness required can easily exceed 100 microns. Copper plating for stud structures requires a similar thickness of photoresist [4]. Extending the microlithographic processes into these rapidly growing areas is placing new demands on both the photosensitive materials and lithography equipment.

Electroplating metals for micro-scale features does not present new technical challenges. However, the fabrication of high aspect ratio linewidths for the applications described above is a new and challenging use of photolithography equipment and photoresists. The photolithography requirements for thick photoresists can be addressed by using optical lithography equipment originally developed for production of semiconductor devices. Steppers, full wafer scanners and contact printers are widely used in the microelectronic industry and are highly evolved production tools. Thick photoresists, however, typically require a high exposure dosage and large depth of focus (DOF) for high aspect ratio lithography of larger geometries. For these reasons, it is advantageous to utilize a stepper with a broad band exposure system and low numerical aperture (NA) to maximize the illumination intensity at the wafer plane and to improve DOF [5].

Until recently, most manufacturers were achieving 65 $\mu$ m coats by coating 3 or 4 subsequent coats. This process requires coating and baking 3 to 4 times with significant delays between coats. This repetitive process increases coat defects, slows throughput, increases resist consumption and ultimately leads to a more expensive process. Additionally multiple coat processes can be very susceptible to resist cracking due to thermal shock and mechanical stresses.

There are benefits to using 1X whole wafer proximity printing for Cu bumping. Equipment costs are much less and masks can be designed to easily accommodate edge exclusion areas. Proximity printers can use masks with iron oxide rather than chrome. This allows through the mask viewing to make alignment easy and eliminates view windows needed for the alignment optics. These view windows will expose the resist and then plate up. This leaves a large area of die loss in two locations on each wafer. Iron oxide masks used with broadband illumination create a problem when using broadband resists such as AZ4620 resist. The iron oxide coating passes sufficient energy in the upper wavelengths to partially expose the resist causing blanket resist loss during develop. Resist thickness loss of 5-10% is common. Additionally the resist loss will be inconsistent mask to mask because of the varying optical density of the iron oxide coatings. The resist being used in this application should be non-sensitive in the wavelengths that iron oxide will pass to avoid exposure in the unintended areas. Chemically amplified resists are ideal for this situation since the PAG (photo acid generators) are usually tuned for one specific wavelength.

Photoresist performance, like stepper performance, has generally been optimized over recent years for achieving the smallest geometries possible. Some newer photoresist formulations are available that have properties more tailored for making the high aspect ratio structures required for electroplating molds. The process operating conditions for thick photoresists are considerably different than for thin photoresists. In the case of thin photoresists, the two primary issues are resolution and latitude [4]. With thick films the concerns are centered around aspect ratios, downstream plating performance, latitudes and productivity. As spin coated photoresist films become more popular for these applications, it becomes important to study thick photoresists for optimization of performance and productivity [5,6,7,8].

Traditionally positive tone resists in the 50 $\mu$ m to 100 $\mu$ m range are very difficult to formulate. For example, it is very difficult to design a positive tone chemistry to achieve the transparency necessary, resulting in ultra-high exposures or poor profiles or no image at all. Furthermore very thick positive novalak resists have the characteristic of popping or void formation after exposure as a result of the

nitrogen generated during exposure. One further item that affects productivity is the need to do multiple coats to achieve thickness of around 65 $\mu\text{m}$ . For these reasons we investigated chemically amplified resists for this application. Chemically amplified resist does not show attributes of poor transparency or voiding, and can achieve 65 $\mu\text{m}$  or greater thickness in one coat. How well the resist performs during plating is critical since plating such high features means the resist can be exposed to very harsh plating environments for an extended time. Photoresist cracking is very common with extended plating times and harsh chemistries.

There are a few more issues associated with choosing the tone (positive or negative) of the resist for very thick plating layers. Traditionally negative resists are very difficult to remove after plating or etching due to their chemical composition. Positive resists do not have this issue. Furthermore the photolithography community has been using positive resists for many years. A certain comfort level is achieved by staying with a positive tone resist. We felt it was important that the resist used for bumping applications in our manufacturing facility be compatible with TMAH developers since this developer is common in the wafer production areas. It has been shown that significant precautions must be taken in order to run TMAH and KOH in the same factory and so we wanted to avoid older resist technologies that require KOH developer.

For the reasons mentioned TriQuint Semiconductor challenged Shin-Etsu to develop a new generation chemically amplified I-line resist for copper bumping. The original goal was for a 65 micron thick film and 50 micron diameter bump feature, since this was considered to be the standard outer limits for a positive tone resist. The resist needed to produce target film thickness in a single coat and be TMAH developable. This resist would also have to hold up to severe plating conditions. Shin-Etsu developed a resist formulation designated SIPR<sup>®</sup> 7120M-20 for TriQuint to test. The purpose of this study was to determine if these parameters could be met using this resist.

## 2.0 EXPERIMENTAL METHODS

### 2.1 Lithography Equipment

Exposures for the thick photoresist evaluated in this study was performed on a Karl Suss MA150 with broadband optics. Figure 1 shows the spectral output. Iron oxide masks were used with an exposure gap of 100 microns. With this exposure gap, mask contact with the wafer is minimized yet the aerial image has sufficient vertical energy and minimal blurring to produce desirable wall profiles. The track equipment used was a Karl Suss ACS200

### 2.2 Photoresist Processing

SEMI standard 150 mm ultra-flat silicon wafers sputtered with 1700 Angstroms of copper were used for this study. The photosensitive material used for this investigation was Shin-Etsu SIPR<sup>®</sup> 7120M-20. This resist has a viscosity rating of 5700cps. Pumping this resist requires specialized equipment designed for high viscosity fluids. The Shin-Etsu SIPR<sup>®</sup> 7120M-20 resist was coated to 100 micron thickness in a single coating using the process and equipment described in Table 1. A prewet of PGMEA was used to minimize the coating defects. This far exceeded the target thickness of 65 microns. Photoresist thickness and uniformity were measured on a DekTak.

Shin-Etsu SIPR<sup>®</sup> 7120M photoresist is a chemically amplified I-line photoresist. The thickness at 300 RPM is 100 $\mu\text{m}$ . It is important to note that the SIPR<sup>®</sup> 7120M is formulated with an elastomer additive to

prevent cracking during plating. Cotton-candy formation during coating is a common issue with thick resists and is usually prevented by optimizing dispense volume, using slower spin speeds, and keeping the spin bowl wet during the casting/spreading steps. The 7120M-20 resist has a nominal thickness of 20 $\mu$ m at 3000 RPM but when spun at slow speeds can achieve thickness exceeding 100 micron in a single coat.

One additional benefit of the elastomers in this resist is to cause the resist to be workable for a relatively long processing time. The coat can be spun to thickness using a slow spin speed over a long period of time and still remain fluid. It will tend to lay down or reflow after spinning. This is why 300 RPM is an acceptable spin speed. For a 100 $\mu$ m coat the uniformity is 5 micron, one sigma. Through a proprietary edge bead reduction process the edge bead thickness is the same as the rest of the coat.

The resist is easily patterned using conventional semiconductor processing. TMAH 0.26 normal with surfactant was used for development. G,H,I-line wavelengths were selected for exposure even though the resist is only sensitive to I line. There was no negative effect noticed with using the three wavelengths. The softbake was done on a track hot plate bake at 100C for 8 minutes followed by an oven bake for 2 hours at 110C. The PEB is 95C for 120 seconds. It was found to be very important to eliminate a lot of the solvent in the thick film to provide good, smooth profiles. Figure 5 shows a resist profile with pitting caused by too much solvent remaining in the film during exposure/develop. The exposure energy is 4500 mJ/cm<sup>2</sup> and the development time is 15 minutes immersion at room temperature, followed by a DI water rinse

## 2.3 Data Analysis

After exposure the wafers were cleaved for cross sections on a Jeol JSM 6400F.

# 3.0 RESULTS AND DISCUSSIONS

## 3.1 Linearity Comparison

Figure 2 shows the process linearity for the SIPR 7120M photoresist at 4500 mJ/cm<sup>2</sup>. This graph shows that the printed feature size is linear with respect to the reticle feature size. It appears to be linear down to approximately 35 $\mu$ m with respect to the bottom C.D. The top C.D. blows out, but becomes notably less at 50 $\mu$ m and above.

Figure 3 shows cross sectional SEM photographs of the process linearity for lines exposed in 100 microns of SIPR 7120M photoresist. All of the linewidths were exposed at 4500 mJ/cm<sup>2</sup> with a proximity gap of 100 microns. The foot at the base of the photoresist is minimal down to the 25 $\mu$ m feature size. The feature top sidewall width increases notably below a 50 $\mu$ m feature size that is most likely attributable to the 100 micron proximity gap used in this study. Overall the goal was greatly exceeded.

One worry was amine contamination of chemically amplified resists. The SIPR 7120M resist was formulated to be insensitive to amines. Exposed wafers were left out in an open photo area for 8 hours and showed no affect to the image. There was no detectable latent image decay up to 24 hours.

The polystyrene resin has proven to be superior to the traditional Novalak with respect to adhesion to Cu seed metal. No surface preparation was required. There has been no loss of adhesion observed during the long plating process.

### 3.2 Plating and Stripping

Figure 4 shows the results of plating. The photos show plated copper features. The CDs are 75 and 150 microns. There were no issues seen with copper plating. The plating resistance and adhesion were shown to be very acceptable for this process. Additionally the stripping of the resist after plating was accomplished using heated NMP in a recirculating bath followed by DI H<sub>2</sub>O rinse. No residue is seen.

## 4.0 CONCLUSIONS

Our original goal when we started this project was to achieve a 50 $\mu$ m feature in 65 $\mu$ m thick resist. The 65 $\mu$ m thickness target is very common for this type of bump process. During our work we determined the capability of this resist went to 100 $\mu$ m thick in a single coat with even better resolution capabilities. The process targets were then very quickly changed. This study has shown the feasibility of processing the Shin-Etsu SIPR 7120M photoresist at 100 $\mu$ m thick with a single coat process on a Karl Suss ACS200. SIPR 7120M is a positive acting, acid catalyzed based material that can be easily processed using conventional semiconductor processing equipment. This photoresist has well balanced lithographic properties, allowing it to be coated and exposed at 100 $\mu$ m in one coat. Full process characterization was shown from coating, patterning, plating and stripping.

A linearity and resolution study was performed to investigate the process latitudes. It was determined that the resolution goal of 50 $\mu$ m was far exceeded by the performance of the SIPR 7120M. The 25 $\mu$ m resolution suggests that SIPR 7120M has the capability of supporting future generations of plating processes as feature sizes decrease and form factor requirements increase. Near vertical sidewalls were also observed, suggesting plated features will meet or exceed expectations. Throughput in regards to wait times, bake times and exposure times was determined to be acceptable as well as far exceeding the performance of standard novalak based resists.

Copper plating performance was checked on blanket focus and exposure copper seed wafers. All plating work was done at TriQuint Semiconductor. No cracking was observed even at 100 $\mu$ m plating thicknesses. Also the resist removed cleanly after plating using warm NMP.

## 5.0 ACKNOWLEDGEMENTS

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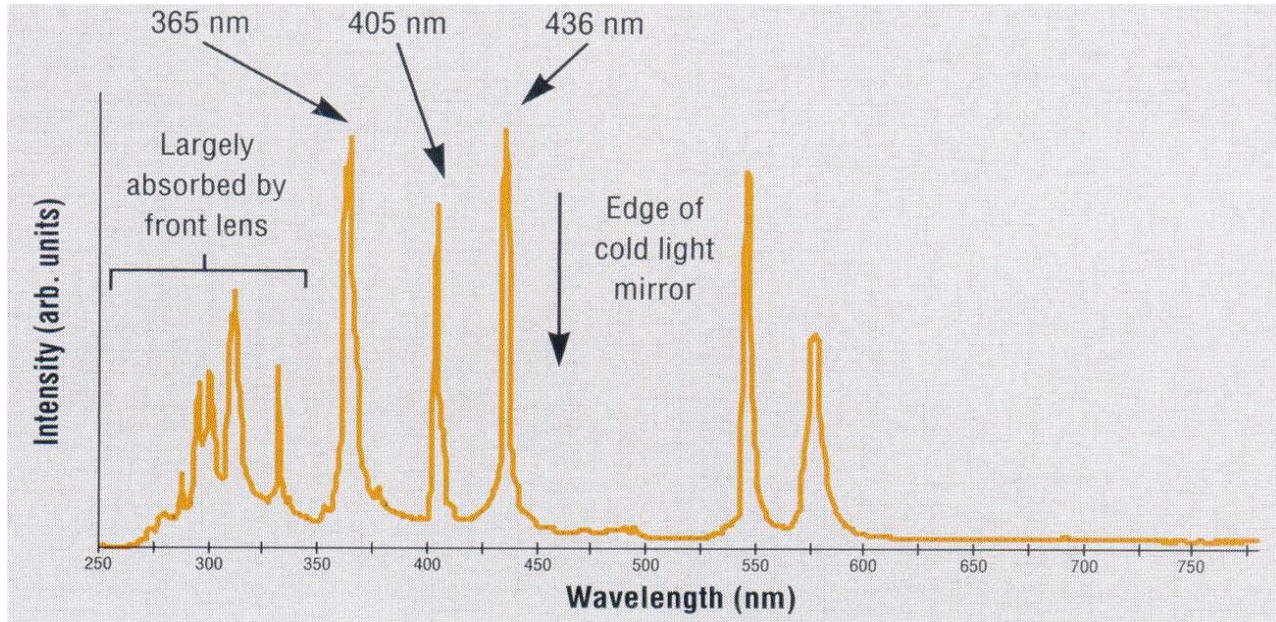


Figure 1: Karl Suss MA 150 spectral output

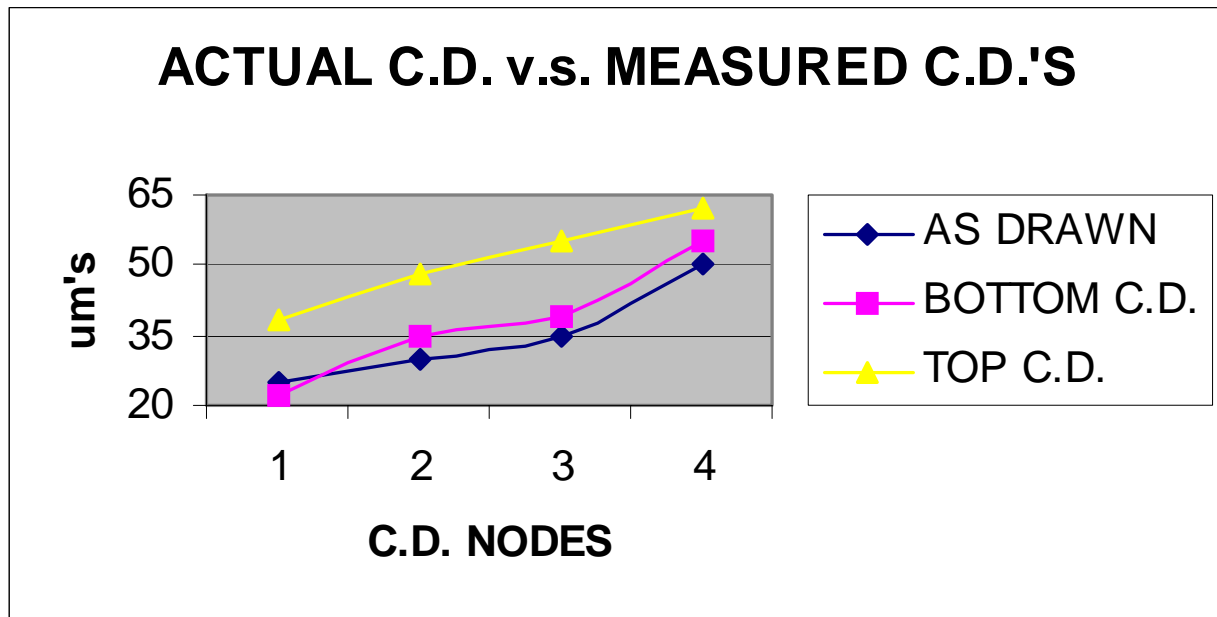
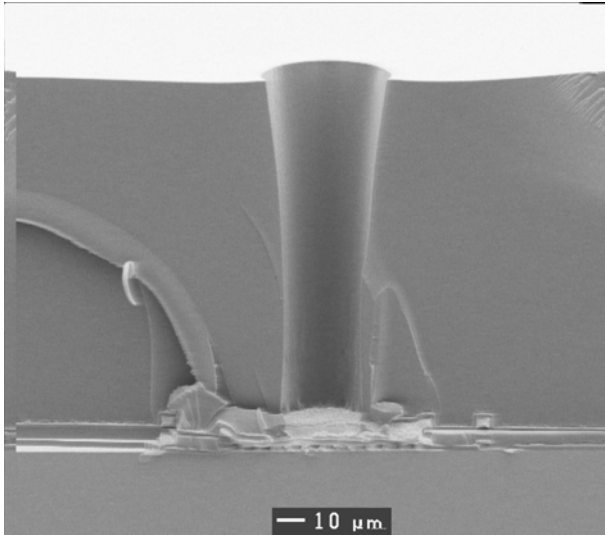
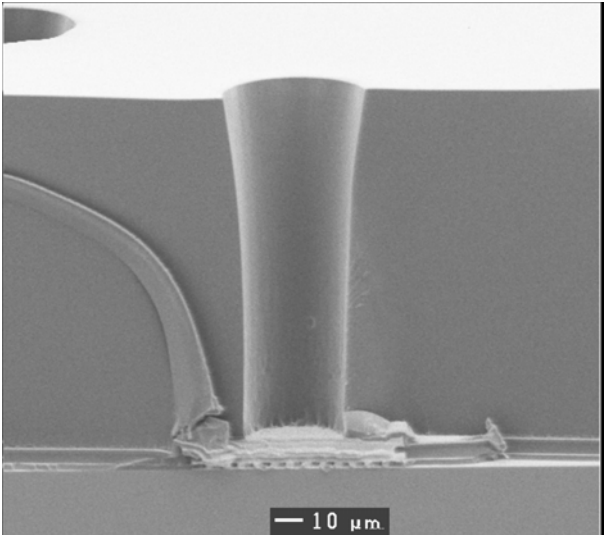


Figure 2: Mask linearity of SIPR 7120 at 100µm thick

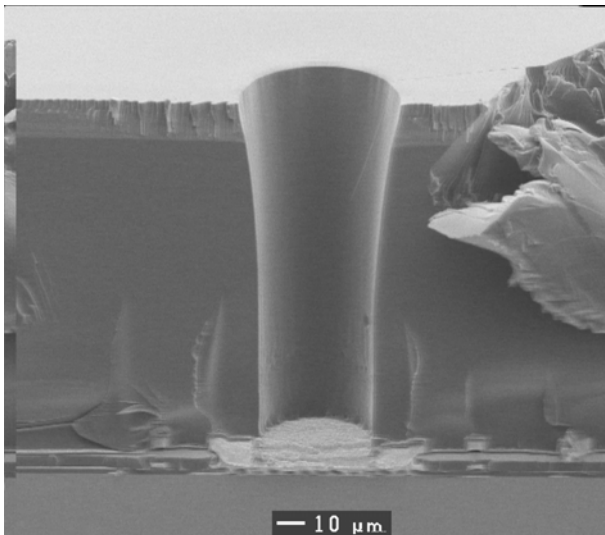
25μm C.D.



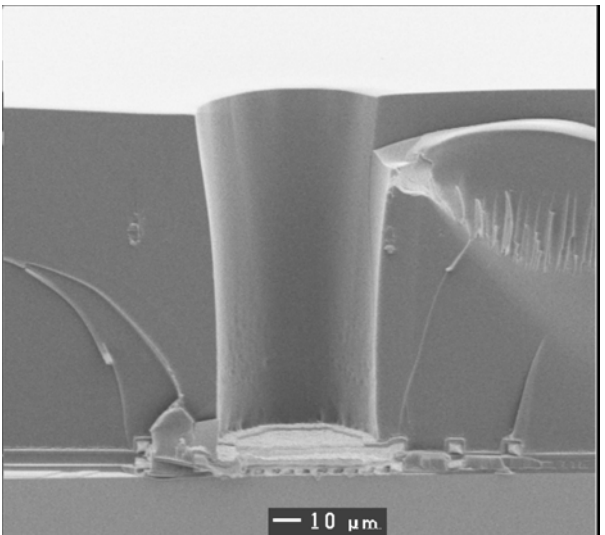
30μm C.D.



35μm C.D.

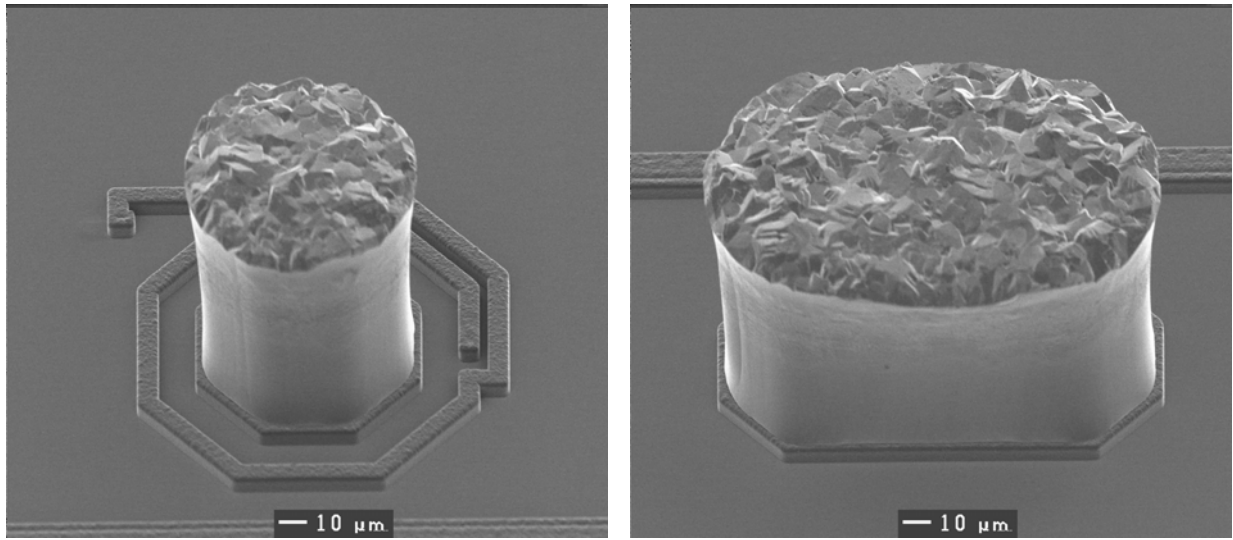


50μm C.D.

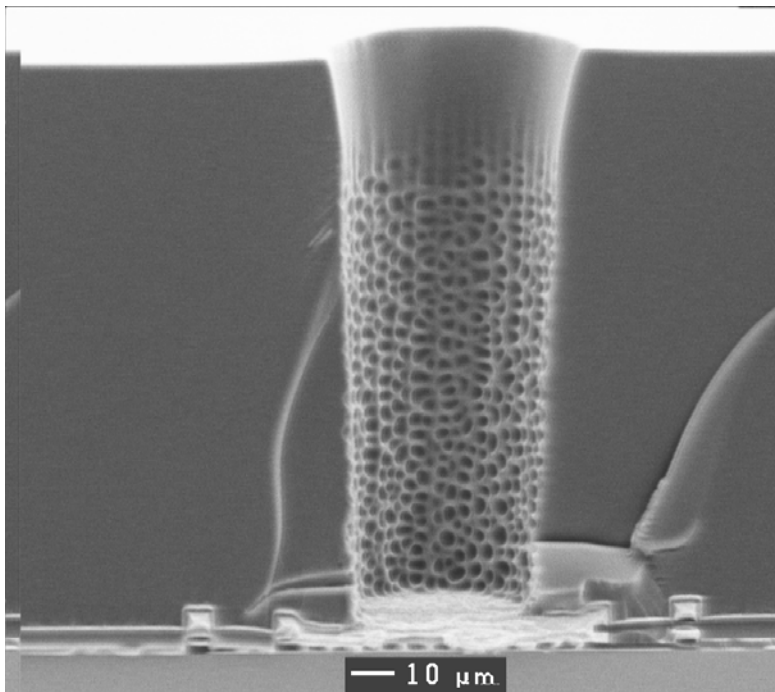


**Figure 3:** SEM cross section photographs of the CD linearity in 100μm thick Shin-Etsu SIPR 7120 after develop





**Figure 4:** Electroplated Cu bumps after resist strip, 75µm and 150µm feature



**Figure 5:** Pitting caused by too much solvent after softbake in 100µm SIPR 7120

PROCESS STEP	PARAMETERS	EQUIPMENT
SIPR-7120M Coat	Solvent pre-wet PGMEA Dynamic dispense photoresist Volume=12cc Spin 45 secs 300 RPM Acetone backwash @ spin	KARL SUSS ACS 200
Softbake	Hotplate 8 minutes @ 100C Oven bake @110C for 2 hours	KARL SUSS ACS 200 Convection Oven
Exposure	4500 m.j. @ 100µm gap	KARL SUSS MA150
PEB	15 Minute wait, 95C 120 seconds	KARL SUSS ACS 200
Develop	15 minutes 0.26 N TMAH	Sink

**Table 1:** Process conditions for Shin\_Etsu SIPR 7120 100µm thickness.